

CLAIMS

Having thus described my invention in detail, what I claim is new, and desire to secure by the Letters Patent is:

1. A method of providing a substantially planar trench isolation region having rounded trench isolation/substrate corners, said method comprising the steps of:

(a) forming a film stack on a surface of a substrate, said film stack comprising an oxide layer, a polysilicon layer and a nitride layer;

(b) patterning said film stack so as to form at least one trench within said substrate, wherein said patterning exposes sidewalls of said oxide layer, polysilicon layer and nitride layer;

(c) oxidizing the at least one trench and said exposed sidewalls of said oxide layer and said polysilicon layer so as to thermally grow a conformal oxide layer in said trench and on said exposed sidewalls of said oxide layer and said polysilicon layer;

(d) filling said trench with a trench dielectric material; and

(e) planarizing to said surface of said substrate.

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1 2. The method of Claim 1 wherein said substrate is
2 composed of Si, Ge, SiGe, GaAs, InAs, InP or a layered
3 semiconductor.

1 3. The method of Claim 1 wherein said oxide layer of
2 said film stack is thermally grown or deposited.

1 4. The method of Claim 3 wherein said oxide layer of
2 said film stack is deposited by chemical vapor deposition
3 (CVD), plasma-assisted CVD, sputtering or evaporation.

1 5. The method of Claim 1 wherein said oxide layer of
2 said film stack has a thickness of from about 5 to about
3 20 nm.

1 6. The method of Claim 5 wherein said oxide layer of
2 said film stack has a thickness of from about 6 to about
3 12 nm.

1 7. The method of Claim 1 wherein said polysilicon layer
2 of said film stack is formed by a deposition process
3 selected from the group consisting of CVD, plasma-
4 assisted CVD and sputtering.

1 8. The method of Claim 1 wherein said polysilicon layer
2 of said film stack has a thickness of from about 25 to
3 about 200 nm.

1 9. The method of Claim 8 wherein said polysilicon layer
2 of said film stack has a thickness of from about 80 to
3 about 120 nm.

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1 10. The method of Claim 1 wherein said nitride layer of
2 said film stack is formed by a deposition process
3 selected from the group consisting of CVD, plasma-
4 assisted CVD, evaporation and sputtering.

1 11. The method of Claim 1 wherein said nitride layer of
2 said film stack has a thickness of from about 50 to about
3 30 nm.

1 12. The method of Claim 11 wherein said nitride layer of
2 said film stack has a thickness of from about 100 to
3 about 200 nm.

1 13. The method of Claim 1 wherein said patterning
2 includes lithography and etching.

1 14. The method of Claim 13 wherein said lithography step
2 includes applying a photoresist to said nitride layer of
3 said film stack, patterning the photoresist by exposure,
4 and developing the pattern in said photoresist.

1 15. The method of Claim 13 wherein said etching step
2 includes a dry etching process selected from the group
3 consisting of reactive-ion etching (RIE), ion-beam
4 etching, plasma etching or any combination thereof.

1 16. The method of Claim 1 wherein said oxidizing is
2 carried out in an oxygen-containing atmosphere at a
3 temperature of about 800°C or above and for a time period
4 of about 30 minutes or less.

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1 17. The method of Claim 16 wherein said oxidizing is
2 carried out at a temperature of from about 900° to about
3 1000°C for a time period of from about 5 to about 10
4 minutes.

1 18. The method of Claim 16 wherein said oxygen-
2 containing atmosphere comprises O₂, ozone, N₂O or mixtures
3 thereof.

1 19. The method of Claim 16 wherein said oxygen-
2 containing atmosphere is admixed with an inert gas, said
3 inert gas being present in an amount of about 90% or less
4 in said mixture.

1 20. The method of Claim 1 wherein said thermally grown
2 oxide layer has a thickness of from about 10 to about 30
3 nm.

1 21. The method of Claim 20 wherein said thermally grown
2 oxide layer has a thickness of from about 18 to about 24
3 nm.

1 22. The method of Claim 1 wherein said filling
2 comprising a deposition process selected from the group
3 consisting of CVD, plasma-assisted CVD and sputtering.

1 23. The method of Claim 1 wherein said trench dielectric
2 material is tetraethylorthosilicate (TEOS), SiO₂, or a
3 flowable oxide.

1 24. The method of Claim 23 wherein said trench
2 dielectric material is TEOS and a densification step is
3 employed prior to said planarizing.

1 25. The method of Claim 1 wherein said planarizing
2 comprises chemical-mechanical polishing or grinding.

1 26. The method of Claim 1 wherein said at least one
2 trench is a deep trench, a moderate trench, a shallow
3 trench or any combinations thereof.

1 27. The method of Claim 26 wherein said at least one
2 trench is a shallow trench.

1 28. A semiconductor device comprising at least one
2 substantially planarized trench isolation region formed
3 within a substrate electrically isolating adjacent active
4 devices regions from each other, said planarized trench
5 isolation region containing rounded corners between the
6 top surfaces of the trench isolation region and the
7 substrate.

1 29. The semiconductor device of Claim 28 wherein said
2 substrate is composed of Si, Ge, SiGe, GaAs, InAs, InP or
3 a layered semiconductor.

1 30. The semiconductor device of Claim 28 wherein said at
2 least one planarized trench isolation region comprises a
3 deep trench isolation region, a moderate trench isolation
4 region, a shallow trench isolation region or any
5 combinations thereof.

1 31. The semiconductor device of Claim 30 wherein said at
2 least one planarized trench isolation region is a shallow
3 trench isolation region.

1 32. The semiconductor device of Claim 28 wherein said at
2 least one planarized trench isolation region includes a
3 thermally grown oxide liner and a trench dielectric
4 material.

1 33. The semiconductor device of Claim 32 wherein said
2 trench dielectric material is tetraethylorthosilicate
3 (TEOS), SiO_2 , or a flowable oxide.

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